What Is Claimed Is:

1. A circuit for receiving data for a synchronous semiconductor memory device, comprising:

a strobe generator having a flip flop and a plurality of logic gates for generating S(n) internal strobes based on an external strobe signal, each of the S(n) internal strobes having a latch-triggering transition occurring one after another in response to the external strobe signal;

a plurality of latches for receiving an n-bit data, including at least one set of latches being clocked by the S(n)th internal strobe and another set of latches for receiving the outputs from the one set of latches, the another set of latches being clocked by an internal clock signal having a period longer than that of an external clock signal ; and

a data write driver for receiving the outputs of the another set of latches and for driving the n-bit data into memory cells of the memory device under clocking control of the external clock.

2. The circuit of claim 1, further including a frequency divider for dividing by two the external clock signal to derive the internal clock signal for clocking the another set of latches.

3. The circuit of claim1, wherein the plurality of latches includes a first set of L(n-1) latches for receiving respective (n-1) bits of an n-bit data, each of the first set of latches being clocked by a respective S(n-1) internal strobe, and a second set of latches configured to receive respective outputs of the first set L(n-1) latches and the nth bit data, the second set of latches being clocked by the S(n)th internal strobe, and a third set of latches for receiving respective outputs of the second set of latches, the third set of latches being clocked by the internal clock signal, the external clock signal being derived from an external memory controller.

4. The circuit of claim 3, further including a frequency divider for dividing by two the external clock signal to derive the clock signal for clocking the third set of latches

5. The circuit of claim 1, wherein the flip flop in the strobe generator is configured as a frequency divider for dividing by two the external strobe signal, and the complementary outputs of the flip flop are applied to the inputs of four AND gates to produce the S(n) internal strobes.

6. The circuit of claim 1, wherein the semiconductor memory device is a double data rate SDRAM.

7. The circuit of claim 1, wherein (n) is equal to four (4).

8. A circuit for receiving data to be written in a synchronous semiconductor memory device, comprising:

a first set of latches for receiving an n-bit data upon transition of an internal strobe signal;

a counter for counting the number of transitions of the internal strobe signal and for outputting an indicating signal upon counting the end of a string of internal strobe signals;

a second set of latches for receiving the outputs of the first set of latches, the second set of latches being clocked by the indicating signal; and

a third set of latches for receiving the outputs of the second set of latches, the third set of latches being clocked by a clock signal derived from a system clock.

9. The circuit of claim 8, wherein the counter is clocked by a first clock derived from the system clock.

10. The circuit of claim 9, wherein the first clock is derived from a falling edge of the system clock.

11. The circuit of claim 9, wherein a counter reset signal is generated based on the falling edge of the system clock after a write command, the counter reset signal for resetting the counter.

12. The circuit of claim 9, wherein the first set of latches receives the n-bit data serially under clocking control by the internal strobe signal.

13. The circuit of claim 8, wherein the second set of latches receives the latched n-bit data in parallel.

14. The circuit of claim 8, wherein the indicating signal is output by the counter upon detecting two transitions of the internal strobe signal.

15. The circuit of claim 8, wherein (n) is equal to four.

16. The circuit of claim 8, wherein the clock signal is derived by dividing by two the system clock.

17. The circuit of claim 8, wherein at least one of the first set of latches serially shifts the first and the third of the n-bit data, wherein (n) equals four.

18. The circuit of claim 8, wherein the internal strobe signal is generated from a falling edge of an external data strobe signal.

19. A circuit for receiving data to be written in a synchronous semiconductor memory device, comprising:

a first set of latches for receiving an n-bit data upon transition of an internal strobe signal;

a counter for counting the number of falling edges of an external strobe signal and for outputting a counting signal;

an indicating signal generator for receiving the counting signal outputted from the counter and for outputting an indicating signal ;

a second set of latches for receiving the outputs of the first set of latches, the second set of latches being clocked by the indicating signal; and

a third set of latches for receiving the outputs of the second set of latches, the third set of latches being clocked by a clock signal derived from a system clock.

20. The circuit of claim 19, wherein the counter is clocked by a first clock derived from the system clock.

21. The circuit of claim 20, wherein the first clock is derived from a falling edge of the system clock.

22. The circuit of claim 20, wherein a counter reset signal is generated based on the falling edge of the system clock after a write command, the counter reset signal for resetting the counter.

23. The circuit of claim 19, wherein the clock signal is derived by dividing by two the system clock.

24. A circuit for receiving data to be written in a synchronous semiconductor memory device, comprising:

a first set of latches for receiving an n-bit data upon transition of a first internal strobe signal buffered from a data strobe buffer;

a counter for counting the number of rising edges of a second internal strobe signal outputted from the data strobe buffer and for outputting a counting signal;

an indicating signal generator for receiving the counting signal outputted from the counter and for outputting an indicating signal ;

a second set of latches for receiving the outputs of the first set of latches, the second set of latches being clocked by the indicating signal; and

a third set of latches for receiving the outputs of the second set of latches, the third set of latches being clocked by a clock signal derived from a system clock.

25. The circuit of claim 24, wherein the counter is clocked by a first clock derived from the system clock.

26. The circuit of claim 25, wherein the first clock is derived from a falling edge of the system clock.

27. The circuit of claim 25, wherein a counter reset signal is generated based on the falling edge of the system clock after a write command, the counter reset signal for resetting the counter.

28. The circuit of claim 24, wherein the clock signal is derived by dividing by two the system clock.

29. A semiconductor memory device for accessing data in synchronization with an external clock signal, comprising:

a converting circuit for outputting at least four bits of serial data as four bits of parallel data in response to a data strobe signal, and

a latch circuit for receiving the four bit of parallel data in response to a first clock signal and outputting the four bit of parallel data to a data write circuit in response to the first clock signal, wherein each of the four bits of parallel data has a valid data window corresponding to at least two clock cycles of the external clock signal.

30. The semiconductor memory device of claim 29, wherein the semiconductor memory device further includes a division circuit for dividing an internal clock signal outputted from a clock buffer to output the first clock signal.

31. A semiconductor memory device for accessing data in synchronization with rising and falling edges of a clock signal, the semiconductor memory device comprising:

a division circuit for generating a second data strobe signal by dividing a first data strobe signal;

a plurality of internal strobe signal generating circuits for receiving the first data strobe signal and the second data strobe signal and generating a plurality of internal strobe signals;

a plurality of first latch circuits for sequentially latching a plurality of received serial data in synchronization with each of the plurality of internal strobe signals;

a second latch circuit for receiving and storing data from the first latch circuit in synchronization with one of the plurality of internal strobe signals; and

an output circuit for receiving data from the second latch circuit in response to a predetermined clock signal, and transferring the received data to a data bus line.

32. The semiconductor memory device according to claim 31, further comprising:

a second division circuit for generating a second clock signal by dividing a first clock signal; and

an output circuit for transferring an output signal of the second latch circuit into a data bus line in response to the second clock signal.

33. A data input circuit for inputting data into a semiconductor memory device comprising:

a converting circuit for converting serial data into parallel data in synchronization with rising and falling edges of a data strobe signal;

a data strobe counter for receiving the data strobe signal and an internal clock signal, for counting the number of pulses of the data strobe signal at an interval where the data strobe signal is enabled, and outputting a count signal corresponding to the number of the pulse signals of the data strobe signal;

a first latch circuit for receiving and latching output data of the converting circuit in response to the count signal; and

a second latch circuit for receiving and latching output data of the first latch circuit in response to the internal clock signal.

34. The data input circuit of claim 33, wherein the data strobe counter receives a write command signal and is initialized in response to a first transition of the internal clock signal after a valid data strobe signal is input.

35. The data input circuit of claim 33, wherein the data input circuit further includes an indicating signal generating circuit for receiving the count signal and outputting an indicating signal for clocking the first latch circuit.

36. The data input circuit of claim 33, wherein the converting circuit comprises:

a third latch circuit for latching odd-numbered data of the serial data in response to the data strobe signal; and

a fourth latch circuit for latching even-numbered data of the serial data in response to the data strobe signal, wherein the count signal is generated by counting the number of falling edges of the data strobe signal at the interval where the data strobe signal is enabled.

37. A data input circuit comprising:

a first latching means comprising a first register for latching first data input in response to a rising edge of a first pulse signal of a data strobe signal, a second register for receiving and latching output data of the first register in response to a falling edge of the first pulse signal, a third register for receiving and storing output data of the second register in response to a rising edge of a second pulse signal of the data strobe signal, and a fourth register for receiving and storing output data of the third register in response to a falling edge of the second pulse signal;

a second latching means comprising a fifth register for latching second data input in response to the falling edge of the first pulse signal of the data strobe signal, a sixth register for receiving and storing output data of the fifth register in response to the rising edge of the second pulse signal of the data strobe signal, and a seventh register for receiving and storing output data of the sixth register in response to the falling edge of the second pulse signal;

a third latching means for storing third data input in response to the rising edge of the second pulse signal of the data strobe signal into the third register through the first register and the second register, storing fourth data input in response to the falling edge of the second pulse signal of the data strobe signal into the sixth register through the fifth register, and receiving and storing data from the fourth register of the first latching means in response to an indicating signal generated in response to the falling edge of the second pulse signal of the data strobe signal;

a fourth latching means for receiving and storing data stored into the seventh register of the second latching means in response to the indicating signal;

a fifth latching means for receiving and storing data stored into the third register of the first latching means in response to the indicating signal; and

a sixth latching means receiving and storing data stored into the sixth register of the second latching means in response to the indicating signal.

38. A data input method for inputting data in a semiconductor memory device comprising the steps of:

converting N bits of serial data into N bits of parallel data in synchronization with a data strobe signal;

transmitting the N bits of parallel data to a first circuit in response to a predetermined signal outputted after the last falling edge of the data strobe signal; and

outputting the N bits of parallel data of the first circuit to a second circuit in response to a clock signal derived from an external clock signal.

39. The data input method of claim 38, wherein the predetermined signal is derived by counting signal generated from a counter.

40. The data input method of claim 38, wherein the clock signal is derived by dividing the external clock signal.